WHAT IS CLAIMED IS:

1. A trace circuit built-in a debugging circuit that is in turn built-in a microcomputer and performs program debugging, said trace circuit tracing data on a bus of said microcomputer according to a bus clock signal and outputting the result to an emulator, said trace circuit comprising:

plural trace buffer memories in which the data on said bus of said microcomputer is stored according to the bus clock signal; and

a control circuit which makes said trace buffer memories store cyclically and in a predetermined order the data on said bus, makes said trace buffer memories output cyclically and in a predetermined order the stored data, wherein the storage of data in and output of data from said trace buffer memories is performed in synchronization with the bus clock signal; and

an output terminal through which the data stored in said trace buffer memories is output to said emulator.

2. The trace circuit according to claim 1, wherein said control circuit checks the number of bits of the data on said bus, and

if the number of bits of the data on said bus is equal to or smaller than a predetermined value, said control circuit makes only some of said trace buffer memories stores

the data on said bus, and makes said trace buffer memories, in which the data is stored, output the data cyclically and in predetermined order.

3. The trace circuit according to claim 2, wherein the predetermined value is 4 bits.

4. The trace circuit according to claim 1 further comprising a bit width conversion circuit provided between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes a bit width of the data to be output from said output terminal based on the bit width acceptable to said emulator.

5. The trace circuit according to claim 1 further comprising output latch circuits in a number equal to the number of said trace buffer memories and provided between respective said trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch the output of said trace buffer memories.

6. A trace circuit built-in a debugging circuit that is in turn built-in a microcomputer and performs program debugging, said trace circuit tracing data on a bus of said microcomputer according to a bus clock signal and outputting

the result to an emulator, said trace circuit comprising:

two trace buffer memories in which the data on said bus of said microcomputer is stored according to the bus clock signal; and

a control circuit which makes said trace buffer memories store cyclically and alternately the data on said bus, makes said trace buffer memories output cyclically and alternately the stored data, wherein the storage of data in and output of data from said trace buffer memories is performed in synchronization with the bus clock signal; and

an output terminal through which the data stored in said trace buffer memories is output to said emulator.

7. The trace circuit according to claim 6, wherein said control circuit checks the number of bits of the data on said bus, and

if the number of bits of the data on said bus is equal to or smaller than a predetermined value, said control circuit makes only some of said trace buffer memories stores the data on said bus, and makes said trace buffer memories, in which the data is stored, output the data cyclically and in predetermined order.

8. The trace circuit according to claim 7, wherein the predetermined value is 4 bits.

9. The trace circuit according to claim 6 further comprising a bit width conversion circuit provided between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes a bit width of the data to be output from said output terminal based on the bit width acceptable to said emulator.

10. The trace circuit according to claim 6 further comprising two output latch circuits provided between respective said trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch the output of said trace buffer memories.